

IN THE SPECIFICATION:

Please amend paragraph number [0001] as follows:

[0001] This application is a continuation of application Serial No. 09/941,092, filed August 28, 2001, now U.S. Patent 6,373,011, 6,373,011 B1, issued April 16, 2002, which is a continuation of application Serial No. 09/713,912, filed November 15, 2000, now U.S. Patent 6,365,861, 6,365,861 B1, issued April 2, 2002, which is a division of application Serial No. 09/520,067, filed March 7, 2000, now U.S. Patent 6,350,959 B1, issued February 26, 2002, which is a continuation of application Serial No. 09/133,338, filed August 13, 1998, now U.S. Patent 6,100,486, issued August 8, 2000, which is a division of application Serial No. 08/785,353, filed January 17, 1997, now U.S. Patent 5,927,512, issued July 27, 1999.

Please amend paragraph number [0010] as follows:

[0010] As described in U.S. Patent Nos. 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify individual ICs. Such methods take place “off” the manufacturing line and involve the use of electrically retrievable ID codes, such as so-called “fuse IDs,” programmed into individual ICs to identify the ICs. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses and anti-fuses in an IC so that when the fuses or anti-fuses are accessed, they output a selected ID code. Unfortunately, none of these methods ~~addresses~~ address the problem of identifying and sorting ICs “on” a manufacturing line.

Please amend paragraph number [0015] as follows:

[0015] In a further embodiment, an inventive back-end test method for separating IC devices in need of enhanced reliability testing from a group of IC devices undergoing back-end test procedures includes: storing a flag in connection with an ID code, such as a fuse ID, associated with each of the IC devices in the group indicating whether each IC device is in need of enhanced reliability testing; automatically reading the ID code of each of the IC devices in the group; accessing the enhanced reliability testing flag stored in connection with each of the

automatically read ID codes; and sorting the IC devices in accordance with whether their enhanced reliability testing flag indicates that they are in need of enhanced reliability testing.

Please amend paragraph number [0017] as follows:

[0017] In a still further embodiment, an inventive method in an IC manufacturing process for testing different fabrication process recipes includes the following: providing first and second pluralities of semiconductor wafers; fabricating a first plurality of ICs on each of the first plurality of wafers in accordance with a control recipe; fabricating a second plurality of ICs on each of the second plurality of wafers in accordance with a test recipe; causing each of the ICs on each of the wafers to permanently store a substantially unique ID code, such as a fuse ID; separating each of the ICs on each of the wafers from its wafer to form one of a plurality of IC dice; assembling each of the IC dice into an IC device; automatically reading the ID code from the IC in each of the IC devices; testing each of the IC devices; and sorting each of the IC devices in accordance with the automatically read ID code from the IC in each of the IC devices indicating that the IC is from one of the first and second pluralities of ICs.

Please amend paragraph number [0021] as follows:

[0021] FIG. 4 is a flow diagram illustrating a conventional procedure in an IC manufacturing process for ~~speed sorting~~ speed sorting ICs;

Please amend paragraph number [0025] as follows:

[0025] FIG. 8 is a flow diagram illustrating a procedure in an IC manufacturing process for ~~speed sorting~~ speed sorting ICs in accordance with a further embodiment of the present invention.

Please amend paragraph number [0040] as follows:

[0040] As shown in FIG. 8, the inventive method for sorting IC devices is also embodied in a method 70 in an IC manufacturing process for sorting IC devices in accordance

with an IC standard, such as speed, that is more stringent than an IC standard that the devices were previously sorted in accordance with. It will be understood that although the method of FIG. 8 will be described with respect to ~~speed sorting~~, speed sorting, the method is applicable to all situations in which ICs previously sorted in accordance with an IC standard, such as speed, need to be sorted in accordance with another, more stringent IC standard. Such IC standards may include, for example, access time, data setup time, data hold time, standby current, refresh current, and operating current.

Please amend paragraph number [0044] as follows:

[0044] On occasion, customers request ICs that meet a more stringent speed standard (e.g., 4 nanoseconds (ns)) than any of the ICs in the various bins 84, 86, and 88 have been graded for. While bin 88, for example, may contain ICs that will meet the more stringent speed standard, the bin 88 cannot be used to supply the customer's request because the ICs in the bin 88 have only been graded (i.e., are guaranteed to meet or exceed) a lower speed standard (e.g., 5ns). Therefore, the present inventive method 70 sorts the ICs in a sort step 92 by reading the fuse ID of each IC, accessing the test data 82, including the ~~speed grading~~ speed grading data, associated with the fuse ID, and comparing the accessed ~~speed grading~~ speed grading data with the more stringent speed standard (e.g., 4ns). Those ICs that fail the more stringent speed standard are directed to a speed graded bin 94, while those ICs that pass the more stringent speed standard are directed to another speed graded bin 96 where they can be used to fill the customer's request. The inventive method 70 thus sorts the ICs in accordance with a more stringent IC standard, such as speed, than they were previously sorted in accordance with the present invention without having to retest the ICs, and thus without reusing valuable testing resources to retest ICs.